

All About the Interface: Do Residual Contaminants at A High-Quality h-BN Monolayer Perylene Diimide Interface Cause Charge Trapping?

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Intrinsic charge transport in molecularly thin organic semiconducting crystals is critically sensitive to the quality of the interfaces required to perform the electrical measurements. Most prominent are the dielectric–semiconductor and semiconductor–metal interface. While impacts from the latter on charge transport can be extracted by four-terminal measurements, the impact of the dielectric interface can only be minimized, typically by utilizing inert dielectrics. Here, it is shown that charge transport in organic field-effect transistors based on the *n*-type small molecule *N*, *N*'-di((*S*)-1-methylpentyl)-1,7(6)-dicyano-perylene-3,4:9,10-bis(dicarboximide) (PDI1MPCN2) can be improved up to one order of magnitude by using hexagonal boron nitride (h-BN) as dielectric, compared to a standard SiO₂ substrate. Using temperature-dependent electrical measurements, the charge-transport properties of devices are systematically analyzed, and high four-terminal mobilities of up to 5.0 cm² V^{−1} s^{−1} are obtained. The high mobility likely stems from decreased charge-carrier trapping at the semiconductor–dielectric interface due to the smooth surface of the inert h-BN. Nevertheless, the temperature dependencies of the mobility, threshold voltage, and interface-state trap density suggest that charge-carrier trapping at the dielectric–semiconductor interface still exists. By comparing the data to transport studies performed on thin air-gapped organic films, it is concluded that an interfacial layer (likely water or solvent residues) between h-BN and the monolayer PDI1MPCN2 causes charge trapping.

1. Introduction

In the quest to characterize intrinsic charge transport processes in organic semiconductors, the impact of extrinsic effects such as contact resistances, nonideal morphology, and external contaminants must be minimized.^[1–3] The semiconductor–dielectric interface is critical for charge transport since traps and surface roughness can hinder efficient charge transport.^[4,5] While the surface roughness is easy to characterize, e.g., with atomic force microscopy (AFM) and its origin can thus be easily identified,^[6] this is highly non-trivial for electrically active traps. Such traps are often related to the influence of the dielectric used in organic field-effect transistors (OFETs), since the dielectric constant and other intrinsic properties can impact the charge transport.^[4,5,7–10] In an effort to reduce trapping (at, e.g., water and other intrinsic or extrinsic traps) at the semiconductor–dielectric interface, typically the surface is passivated by the use of self-assembled monolayers (SAMs).^[11] Recently also intrinsically inert hexagonal

boron nitride (h-BN) has been used as a dielectric with the goal to realize a trap-free interface.^[12–14]


In this report, we investigate charge transport in PDI1MPCN2 (*N*, *N*'-di((*S*)-1-methylpentyl)-1,7(6)-dicyano-perylene-3,4:9,10-bis(dicarboximide) (see inset of **Figure 1a**). PDI1MPCN2 is an organic small molecule, which stands out due to good processability via a solution-based crystallization method as well as its excellent *n*-type charge-transport properties.^[15] However, it was recently discovered that potentially electron–phonon scattering or trapping at the OSC–Al₂O₃ dielectric interface limits the charge-carrier transport at elevated temperatures and high charge-carrier densities.^[4] One method to reduce scattering and trapping of charge carriers at the interface is to design air-gap FETs and thereby remove the OSC–dielectric interface completely, which was first used by Podzorov et al. and Menard et al. for freestanding bulk single-crystal OFETs.^[16,17] This approach was also realized in our group by Schaffroth et al.^[18] with air-gap FETs based on a freely suspended PDI1MPCN2 thin film, which constitutes the first realization of this technique with van der Waals bound OSC films down to nanometer thickness. As a consequence, the charge-carrier trapping was reduced significantly, however, the overall mobilities of the freely suspended films were lower than the films in direct contact with

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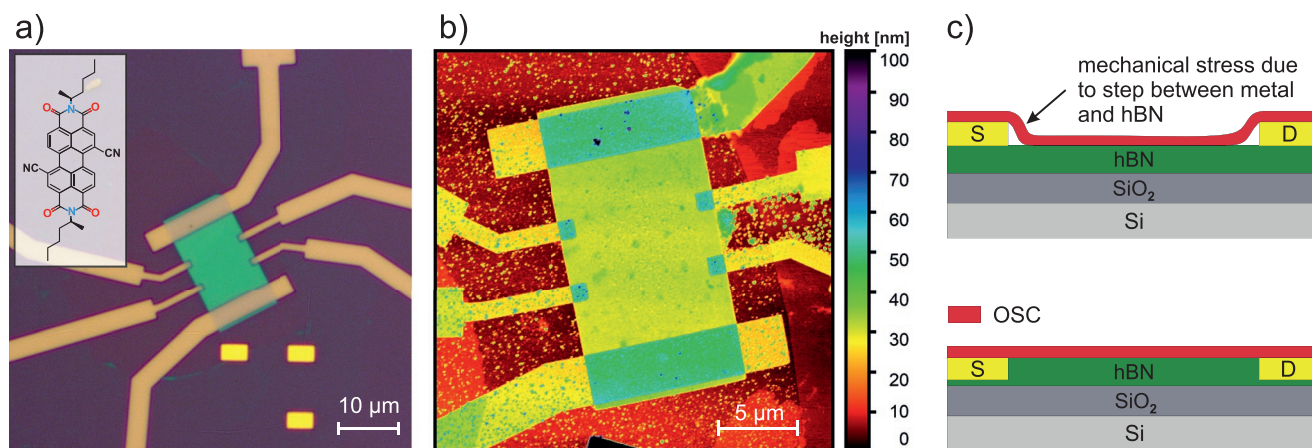


Figure 1. Fabrication of OFET-devices with PDI1MPCN2 on an h-BN dielectric. a) Optical image after h-BN flakes are etched into rectangular shape and metal contacts are ingrained into the h-BN. Inset: structural formula of the PDI1MPCN2 molecule used in this work. b) Atomic force microscope (AFM) image of an OFET device after the PDI1MPCN2 is solution deposited. c) To reduce contact effects, the metal leads are ingrained into the h-BN.

a dielectric, most probably due to contact effects. Another way to improve the OSC-dielectric interface that we want to follow here is to introduce h-BN as the gate dielectric in OFETs. h-BN is a van der Waals material that consists of layers of alternating boron and nitrogen atoms arranged in a hexagonal honeycomb lattice. It has a very smooth and continuous surface relatively free of charge traps and dangling bonds. This makes h-BN a highly inert dielectric, meaning that it exerts less traps and scattering sites on carriers moving in the accumulation channel at the OSC-dielectric interface compared to, e.g., SiO₂ dielectrics. Furthermore, it has a large bandgap that makes h-BN a prime candidate for the gate dielectric in OFET devices.^[19] h-BN was previously used with great success in conjunction with graphene, as the highest mobilities in graphene were measured in graphene-h-BN heterostructures due to the negligible amount of defects and the atom-scale roughness of h-BN.^[13,20,21] In recent years, it was reported that an improvement of charge-transport properties can also be reached in organic semiconductors by using h-BN as gate dielectric and thereby reducing the amount of scattering and trapping at the OSC-dielectric interface.^[12–14,22] This implies that h-BN might allow to realize devices with extremely small interface-state trap density, as obtained before with suspended organic semiconductors, but now with the high mobilities seen on solid dielectrics.

2. Device Fabrication

To investigate the charge transport of PDI1MPCN2 on an h-BN dielectric, bottom gate bottom contact (BGBC) FETs and four-point contact devices were prepared on highly doped silicon substrates with a 300 nm SiO₂ insulator. h-BN flakes, synthesized as described previously,^[23] were exfoliated on top and etched into a rectangular shape (see Figure S1, Supporting Information) using inductively coupled plasma – reactive ion etching (Plasma Lab System 100, Oxford). Since the monolayer PDI1MPCN2 film is only ≈2 nm thin, we can assume that no charge transport occurs over the edges of the h-BN flakes, whose thickness

between 15 and 50 nm lead to a bend in the OSC film inhibiting charge transport.^[15] Consequently, the h-BN flake defines the channel width. Due to the delicate nature of our devices on a micrometer lengthscale, it is not possible to pattern the PDI thin film exactly onto the h-BN flake, since the required lithography procedures would destroy the organic film. As a result, fringe currents around the h-BN flake might impact our electrical measurements as recently discussed by Pei et al.,^[24] where a mobility overestimation of up to 60% in solution processed OFETs was recorded. While we cannot exclude a slight impact of fringe currents on our measurements, we think that a possible mobility overestimation is not nearly as grave as described in ref. [24] due to the reasons outlined in detail in Supporting Information S2. Metal contacts were ingrained into the h-BN as shown in Figure 1 by etching the desired structures into the h-BN before the metal evaporation. Ingraining the contacts provides a rather flat surface without large steps between the metal and the h-BN (Figure 1c). A large step would result in mechanical stress and bad alignment of the organic film and the metal, which leads to a reduced charge-carrier injection and large contact resistances. Keeping the interface on the same level enables a smooth, highly crystalline PDI1MPCN2 thin film, which is applied via a solution-based surface-mediated crystallization process as described in ref. [15]. An atomic-force microscope (AFM) image of a complete device is shown in Figure 1b.

3. Results and Discussion

To investigate the charge transport properties of PDI1MPCN2 on h-BN, two- and four-point measurements were performed in a vacuum point-probe station (CRX-VF Probe Station, Lake-Shore Cryotronics). Annealing of the samples at 400 K for 1–2 days inside the probe station at 3×10^{-7} mbar improved the quality of the samples and is reflected by a more than doubled charge-carrier mobility (see Figure S3, Supporting Information). Transfer curves in the linear and saturation regime of an exemplary annealed sample measured at room temperature

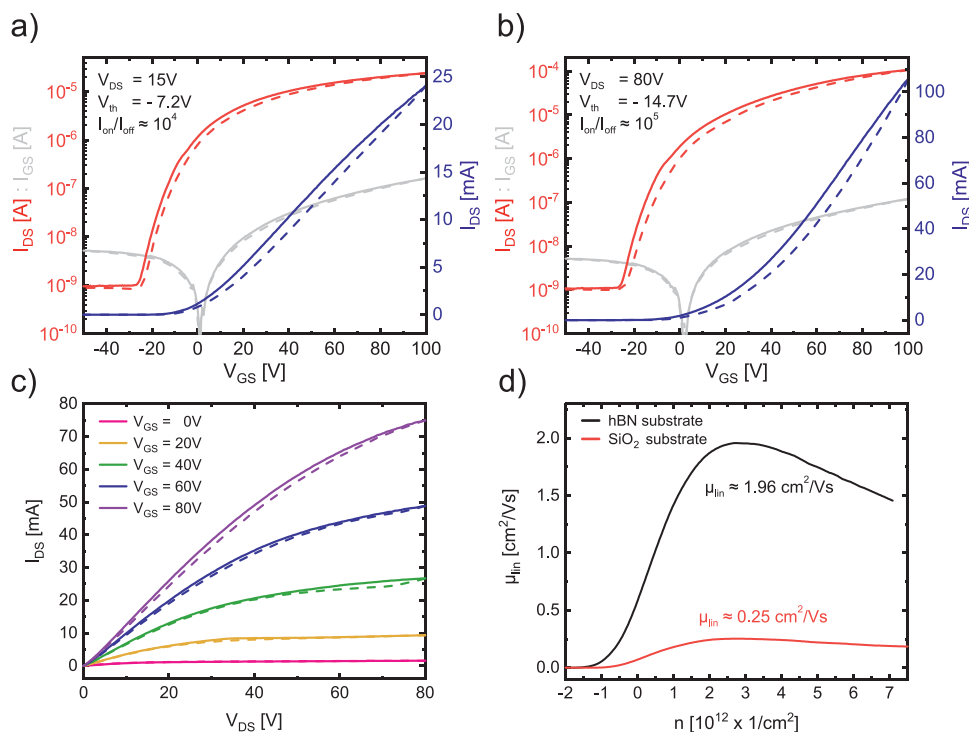


Figure 2. Electrical characterization of PDI1MPCN2 thin films on h-BN at room temperature. a, b) Transfer curves and extracted parameters in the linear (a) and saturation regime (b). The V_{GS} sweep rate is 2 V s^{-1} . c) Corresponding output curve with V_{DS} sweep rate of 4 V s^{-1} . d) Comparison of the linear regime mobilities measured from a device with PDI1MPCN2 on h-BN and PDI1MPCN2 on pure SiO_2 .

are shown in **Figure 2a, b**, respectively, and the corresponding output curve in **Figure 2c**. We observe characteristic electron-transport behavior with an onset voltage slightly below $V_{on} = -20 \text{ V}$ as well as high On/Off-current ratios of approximately $I_{on}/I_{off} = 10^5$ in the saturation regime. Furthermore, the device shows a small hysteresis and a threshold voltage of $V_{th} \approx -7 \text{ V}$. The charge-carrier mobility of $\mu_{lin} = 2.0 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was extracted from the linear-regime transfer curve shown in **Figure 2a**. Additionally, we determined $r_{lin} = 0.89$ as the measurement-reliability factor as proposed by Choi et al.,^[25] which confirms the high quality of the devices. A slightly higher mobility of $\mu_{sat} = 2.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and a corresponding reliability factor of $r_{sat} = 0.90$ was extracted from the saturation-regime transfer curve. The mobilities obtained from different devices were consistently around this magnitude with a maximum value of the linear mobility at room temperature of $\mu_{lin} = 2.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and a corresponding reliability factor of $r_{lin} = 0.77$ (**Figure S4**, Supporting Information).

To analyze the impact of h-BN as a substrate on the charge-carrier transport, we also performed measurements with PDI1MPCN2 on a pure silicon substrate without the additional h-BN layer (**Figure S5**, Supporting Information). In **Figure 2d**, the mobilities from devices with and without h-BN layer are displayed as a function of charge carrier density n , which was determined from the gate voltage, the threshold voltage and the dielectric capacitance per unit area of the substrate as $n = C_{Diell}(V_{GS} - V_{th})/e$. The mobilities from devices with additional h-BN layer show consistently higher mobilities of approximately one order of magnitude, which indicates that the charge-carrier transport is significantly improved by using h-BN as a dielectric substrate.

We further realized a full encapsulation of PDI1MPCN2 between h-BN layers by stamping a second h-BN flake on top of the OFET device, which however—unlike, e.g., in graphene devices—did not result in a further improvement of the charge-carrier transport, possibly due to damaging of the organic thin film during the stamping process (**Figures S6–S9**, Supporting Information).

To shed more light on the impact of the h-BN on the electronic properties of the OSC, we performed a systematic study of the temperature dependent charge transport. The corresponding linear-regime mobilities extracted from the transfer curves displayed in **Figure S10** (Supporting information) are presented in **Figure 3a, b**. The measurements show a freeze out of μ_{lin} at cryogenic temperatures and an almost linear increase with temperature from $T = 100 \text{ K}$ to $T = 260 \text{ K}$, which is followed by a significant drop of μ_{lin} at temperatures above 340 K . While μ_{lin} is largely independent of the charge-carrier density below room temperature, its decrease at high temperatures appears to be more sizeable at higher charge-carrier densities. The same trends can be observed from the transfer curves detected in the saturation regime (**Figure S11**, Supporting Information).

Additionally, we evaluated the activation energy E_a from the linear-regime mobilities following an Arrhenius approach (**Figure 3c**) to values between $E_a = 25 \text{ meV}$ and $E_a = 30 \text{ meV}$, which are in perfect agreement with the results obtained by Vladimirov et al.^[26] for the same molecule when using a SAM-modified Al_2O_3 dielectric.

Besides the temperature dependence of μ , we also investigated the evolution of the threshold voltage V_{th}

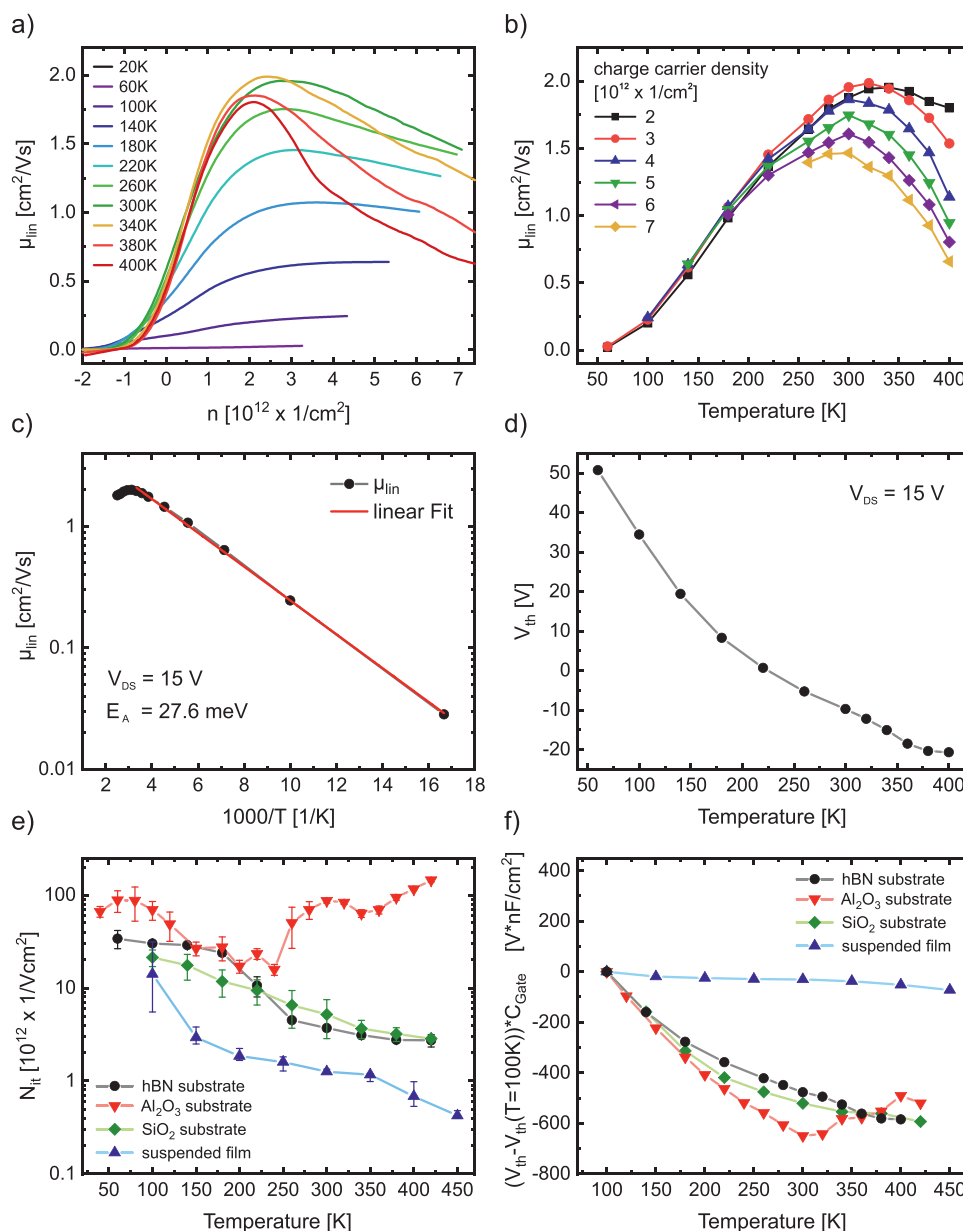


Figure 3. a,b) Temperature dependence of the linear-regime mobility displayed as a function of charge-carrier density (a) and temperature (b). Both plots display a mobility attenuation at elevated temperatures, which is more pronounced at high charge-carrier densities. c) Extraction of the activation energy through an Arrhenius approach. d) Temperature dependent shift of the threshold voltage V_{th} . e, f) Comparison of the temperature dependence of the threshold voltage (e) and interface state trap density between different substrates. The data for suspended films in (e) and (f) were taken from Schaffroth et al.^[18] and measurements for the Al₂O₃ substrate are taken from Vladimirov et al.^[4]

with temperature, as well as the interface-state trap density N_{it} , which was calculated from the subthreshold slope S ($N_{it} = [S \cdot \log(2.718)/(k_B T/e) - 1] C_{diel}/e$ with $S = dV_{GS}/d\log(I_{DS})$, C_{diel} the capacitance per unit area of the gate dielectric, e the elementary charge and k_B the Boltzmann constant).^[4,27,28] Both, V_{th} and N_{it} , show a monotonous decrease with rising temperature (Figure 3d,e). While the magnitude of V_{th} varied between different samples, the overall monotonous temperature development was the same for each sample.

We further compared our values of V_{th} and N_{it} with the results obtained by some of us earlier (Vladimirov et al.^[4] and

Schaffroth et al.^[18]) on the same OSC but using a different dielectric and different solvent for OSC deposition, to gain a deeper understanding of the impact of the different substrates in the OFET device. Since the gate capacitances C_{diel} of the dielectrics differ, it is not sensible to compare V_{th} directly. Rather, the gate-capacitance normalized threshold voltage was evaluated (i.e., $V_{th}^{Norm} = (V_{th} - V_{th}(T=100K)) \cdot C_{diel}$), which allows us to compare the temperature development of V_{th}^{Norm} between different substrates (see Figure 3f). V_{th}^{Norm} obtained from measurements with PDI1MPCN2 located on solid substrates shows a significant temperature dependence, whereas the measurements by

Schaffroth et al.^[18] with a suspended film display a substantially smaller effect of the temperature onto V_{th} , which indicates a larger presence of deep traps when using a device with a solid dielectric. This hypothesis is also supported by the interface state trap density N_{it} , where a lower absolute value of N_{it} on suspended films is observed compared to devices with a solid dielectric (Figure 3e).

Taken together, the measurements of N_{it} , V_{th}^{Norm} , and μ on different dielectrics allow to make suggestions about the underlying phenomena responsible for the observed temperature dependencies. We first turn to the discussion of the possible cause for the decrease of μ at temperatures above 300 K, which seems to be independent of the dielectric used, i.e., h-BN or SiO₂ in the present study, and—in consideration of our earlier work—Al₂O₃.^[4] This decrease might be either related to yet unknown intrinsic effects within the OSC at such high charge carrier densities, or more likely to the dielectric–semiconductor interface, which is also indicated by the measurements of Schaffroth et al. on interface-free air gap OFETs, where no decrease of μ at high temperatures was measured.^[18]

We believe that two possible scenarios are able to explain the observed decrease as was previously hypothesized by Vladimirov et al.^[4] In the first scenario scattering between the charge carriers and phonons in the underlying dielectric is responsible for the deterioration of the mobility. With rising temperature the number of dielectric phonons increases, thus resulting in an increased amount of scattered charge carriers and a reduction in mobility. In the second scenario traps located directly at the OSC–dielectric interface are considered. Depending on their depth, traps can be differentiated between deep and shallow traps. Shallow traps are known to decrease the mobility, whereas deep traps generally only impact the threshold voltage, since the charge carriers are trapped permanently and consequently do not contribute to the charge transport and the mobility.^[4,16,29,30] Possibly, at elevated temperatures the thermal energy is high enough to excite carriers out of the deep traps, effectively turning the deep traps into shallow traps, which leads to the observed decrease in mobility. In both scenarios, the increased attenuation at higher charge-carrier densities displayed in Figure 3a,b can be attributed to the increased gate bias pulling the charge carriers closer to the OSC–dielectric interface, which makes the charges more susceptible to both, scattering and trapping processes.

Consequently, the observation of similar temperature-dependent damping of μ in our samples suggests that scattering or trapping at the OSC–dielectric interface is still existent when using h-BN as a dielectric. The physical origin of these traps or scattering sites—since observed on h-BN, SiO₂, and Al₂O₃ dielectrics—might be a universal interfacial layer, potentially related to solvent residues or water. Recent reports state that water as well as other polar molecules at the OSC–dielectric interface can act as traps localizing charge carriers.^[31–36] In fact, it is known that on any type of surface, several monolayers of water remain and likely are also present on the h-BN dielectrics before and after OSC deposition. For instance, in h-BN encapsulated graphene devices interfacial contaminants had to be removed by mechanical pressing before high mobilities could be observed,^[37] a process we cannot perform using OSCs due to their mechanical properties. Mobility limitations due to

an interlayer could also be the reason that we do not find a dramatic improvement in μ when changing from the Al₂O₃ + SAM dielectric^[4,15] to an h-BN dielectric (here the 4-point mobility (Figure 4e,f) obtained from our devices in bottom-contact geometry should be compared to the top-contact geometry used by Vladimirov et al.^[4] on the Al₂O₃ substrates).

The temperature evolution of V_{th} and N_{it} also points to the presence of external effects, most likely also related to the OSC–dielectric interface. In detail, in our measurements on h-BN and SiO₂, we observe a monotonous decrease of V_{th} and N_{it} (Figure 3e,f) similar to the temperature evolution of the suspended films.^[18] Since the absolute values of V_{th}^{Norm} and N_{it} are significantly smaller in the suspended films, the observed V_{th} and N_{it} on h-BN, SiO₂, and Al₂O₃ dielectrics must stem from effects not related to the OSC itself. Additionally, the h-BN dielectric is extremely inert and trap-free, and therefore unlikely the reason for the high V_{th}^{Norm} and N_{it} values. Consequently, we anticipate that also the deep traps dominating V_{th} and N_{it} are located at the OSC–dielectric interface. Again, trapped solvent or water might be the physical origin of these traps. Trapped solvent or water could—besides other effects discussed in ref. [4]—also explain the different temperature evolutions of V_{th} and N_{it} in the devices prepared on Al₂O₃, if we take into account that the OSC onto Al₂O₃ had been deposited from a dimethyl phthalate : toluene (DMP:Tol) mixture, while in the prior work we only used DMP.

To solidify that effects related to the interface and not other external effects, such as contact resistance, are causing the discussed temperature dependencies, we have also employed four-point measurements. Figure 4a shows the total channel resistance R_{Total} , the contact resistance $R_{Contact}$, as well as the film resistance R_{Film} as function of the gate voltage. The contact resistance accounts for the resistance at both, the source and drain electrode, and is calculated as $R_{Contact} = R_{Total} - R_{Film} = V_{DS}/I_{DS} - L/D \times V_{ap}/I_{DS}$, where V_{ap} is the voltage measured between the probes inside the channel, D is the edge-to-edge distance between those probes, L is the overall channel length, and V_{DS} and I_{DS} are the voltage and the current measured over the whole channel length between the outer contacts, respectively.^[38]

At low gate voltages, the overall resistance R_{Total} is dominated by $R_{Contact}$, since for $|V_{GS} - V_{th}| < |V_{DS}|$ the transistor is in the saturation regime and pinchoff occurs, which leads to a high resistance depletion region at the drain electrode.^[2,3] As V_{GS} increases, both R_C and R_{Film} decrease, likely due to an increased charge-carrier density that results in an increasing semiconductor conductivity. At high gate voltages, the magnitude of $R_{Contact}$ is slightly below the film resistance, however, both resistances are still in the same order of magnitude, which suggests that contact effects might influence measurements in our device.

We have also investigated the temperature dependence of our 4-point devices, and the resulting contact and film resistance are displayed in Figure 4c,d in intrinsic units as width-normalized contact resistance $R_{Contact}W$ and film sheet resistance $R_{Sheet} = R_{Film}(W/D)$. Both resistances show a minimum between $T = 300$ K and $T = 360$ K and increase significantly at low temperatures, presumably due to a freeze out of charge carriers.

When comparing the relation between $R_{Contact}$ and R_{Film} (see Figure 4b) at a fixed gate voltage $V_{GS} = 80$ V, it can be observed

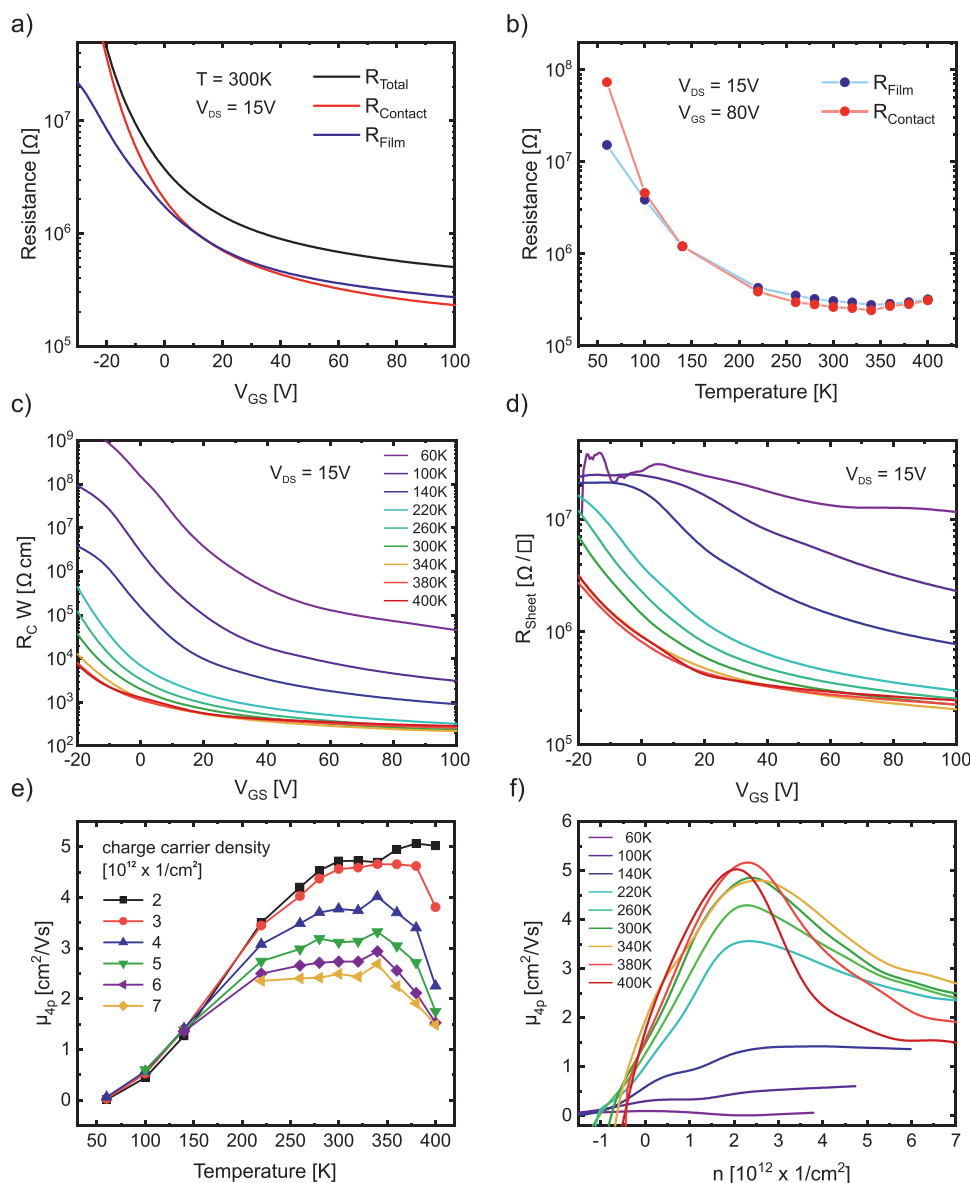


Figure 4. a) Overall channel resistance R_{Total} , contact resistance R_C and film resistance R_{Film} as a function of gate voltage. b) Plot of $R_{Contact}$ and R_{Film} at fixed gate voltage $V_{GS} = 80\text{ V}$ as a function of temperature. At cryogenic temperatures, the contact resistance is dominant, whereas at elevated temperatures $R_{Contact}$ is slightly smaller than R_{Film} . c, d) Width-normalized contact resistance $R_{Contact}W$ (c) and film sheet resistance $R_{Sheet} = R_{Film}(W/D)$ (d) at various temperatures as a function of the gate voltage. e, f) Contact-resistance corrected four-point mobility as a function of the temperature (a) and charge-carrier density (b).

that $R_{Contact}$ is consistently slightly smaller than R_{Film} at elevated temperatures, whereas at lower temperatures $R_{Contact}$ is larger. The more significant increase with decreasing temperature suggests that the impact of contact effects on our device is larger at cryogenic temperatures, which is also supported by the detected output curves. We observe close to ideal output characteristics at room temperature, while nonlinearities and an S-swing can be noticed at low temperatures, which indicates charge-carrier injection problems in our device (Figure S12, Supporting Information).

Finally, we calculated the four-point mobilities $\mu_{lin, 4p} = (D/WC_{Diel})[d(I_{DS}/V_{4p})/dV_{GS}]$, which yield the contact-

effect corrected mobility of our devices (see Figure 4e,f, the corresponding two-point measurements are shown in Supporting Information S13).^[25,38] We use the edge-to-edge distance D in this calculation, to avoid a mobility overestimation due to the impact of the voltage probes inside the accumulation channel, as recently reported by Choi et al.^[39] Using the edge-to-edge distance between the inner voltage probes represents the ultimate shunting scenario described by Choi et al.^[39] and makes sure that we do not risk an overestimation of $\mu_{lin, 4p}$. Figure 4e,f displays the four-point mobilities and similar to the results shown in Figure 3a,b, we observe a density-dependent dampening of the mobility at high temperatures. However, the

absolute mobility values are significantly larger by up to a factor of two, reaching mobilities as high as $\mu_{lin, 4p} = 5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. This indicates that contact effects still impact the measurements in our device, thereby leading to a reduced mobility in two-point measurements. However, the overall temperature-dependent characteristics of the charge-carrier mobility discussed before are the same, confirming that the temperature evolution of μ , V_{th} , and N_{it} are not dominated by contact resistances.

4. Conclusion

We investigated the effect of the van der Waals material h-BN on the charge transport properties of the small molecule *n*-type semiconductor PD11MPCN2 by performing electrical measurements with the inert h-BN as dielectric and comparing them to previous measurements on samples using a conventional substrate, as well as devices with a freely suspended OSC film.^[4,15,18] To exclude contact effects from our results, we employed four-point measurements and observed that while contact resistances influence our measurements in terms of a reduced mobility, the overall temperature-dependent evolution of μ , V_{th} , and N_{it} is not affected. Maximum linear-regime mobilities of $\mu_{lin} = 2.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ from two-point measurements and $\mu_{lin, 4p} = 5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ from four-point measurements reveal a significant improvement of the charge-carrier transport when using h-BN as dielectric, with mobilities being one order of magnitude higher compared to devices with a SiO_2 substrate. We believe that charge-transport improvement stems from decreased charge-carrier trapping at the OSC-dielectric interface, due to the smooth and continuous surface of h-BN. However, a decrease of the mobility μ at elevated temperatures and increased charge-carrier densities suggests that charge-carrier trapping in shallow traps still exists, possibly due to an interfacial layer, which is independent from the dielectric in use and related to solvent residues or water. This hypothesis is further reinforced by investigating the threshold voltage V_{th} as well as the interface-state trap density N_{it} , which are significantly higher in devices with solid dielectrics than in the interface-free suspended films,^[18] indicating that the amount of deep traps is also related to an interfacial layer (likely water or solvent residues) at the OSC-dielectric interface. Further investigations will be required to pinpoint the exact nature of these interfacial contaminants so that they can be removed effectively. Due to the nanoscopic amount of material present at the interface, its identification will require detailed scattering techniques, e.g., at synchrotron sources. Avoiding the contaminants will be particularly challenging since nanoscopic water layers at surfaces are—even in high vacuum environments—hard to remove.^[33] While we have investigated only a specific monolayer semiconductor, it is likely that such a residual water layer also limits device performance in other monolayer and multilayer OFETs and that inert dielectrics are potentially not the final solution to remove all interfacial contaminants.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

charge transport, field-effect transistor, interface, organic semiconductor, van-der-Waals

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